Claim Amendments

Please amend claims 1, 4, 5, 6, 8, and 11-13 as follows:

Listing of Claims

What is claimed is:

1. (currently amended) A field effect transistor (FET) device with enhanced performance within a decreased substrate area comprising:

a semiconductor substrate;

a gate electrode formed over the semiconductor substrate to cover and define a channel region within the semiconductor substrate; and

a pair of source/drain regions formed within the semiconductor substrate and separated by the channel region within the semiconductor substrate, wherein at least one of:

an interface of the channel region covered by the gate electrode, said corrugated interface comprising rounded valley bottom portions; and

an upper surface of the gate electrode, is corrugated.

2. (original) The field effect transistor (FET) device of claim 1

wherein the field effect transistor (FET) device is selected from the group consisting of metal oxide semiconductor field effect transistor (MOSFET) devices and metal semiconductor field effect transistor (MESFET) devices.

3. (previously presented) The field effect transistor (FET) device of claim 1 wherein the at least one of:

the interface of the channel region covered by the gate electrode; and

the upper surface of the channel region covered by the gate electrode, is corrugated with a peak-to-peak longitudinal periodicity of from about 0.02 to about 0.4 microns and a peak-to-valley vertical depth of from about 100 to about 1000 angstroms.

4. (currently amended) A field effect transistor (FET) device comprising:

a semiconductor substrate;

a gate electrode formed over the semiconductor substrate to

cover and define a channel region within the semiconductor substrate; and

a pair of source/drain regions formed within the semiconductor substrate and separated by the channel region within the semiconductor substrate, wherein an interface of the channel region covered by the gate electrode is corrugated, said corrugated interface comprising rounded valley bottom portions and peak portions.

5. (currently amended) A field effect transistor (FET) device comprising:

a semiconductor substrate;

a gate electrode formed over the semiconductor substrate to cover and define a channel region within the semiconductor substrate; and

a pair of source/drain regions formed within the semiconductor substrate and separated by the channel region within the semiconductor substrate, wherein an upper surface of the gate electrode is corrugated, said corrugated surface

comprising rounded valley bottom portions.

6. (currently amended) The field effect transistor (FET) device of claim 1 wherein both the interface of the channel region covered by the gate electrode and the upper surface of the gate electrode are corrugated, said corrugated interface and said corrugated surface comprising rounded valley bottom portions and rounded peak portions.

7. (original) The field effect transistor (FET) device of claim 1 wherein the gate electrode is formed to a thickness of from about 500 to about 2000 angstroms.

8. (currently amended) A method for forming a field effect transistor (FET) device comprising:

providing a semiconductor substrate;

forming over the semiconductor substrate to cover and define a channel region within the semiconductor substrate a gate electrode; and

forming within the semiconductor substrate and separated by

the channel region within the semiconductor substrate a pair of source/drain regions, wherein at least one of:

an interface of the channel region covered by the gate electrode, said corrugated interface comprising rounded valley bottom portions; and

an upper surface of the gate electrode, is corrugated.

9. (original) The method of claim 8 wherein the field effect transistor (FET) device is selected from the group consisting of metal oxide semiconductor field effect transistor (MOSFET) devices and metal semiconductor field effect transistor (MESFET) devices.

10. (previously presented) The method of claim 8 wherein the at least one of:

the interface of the channel region covered by the gate electrode; and

the upper surface of the gate electrode, is corrugated with a peak-to-peak longitudinal periodicity of from about 0.02 to about 0.4 microns and a peak-to-valley vertical depth of from about 100 to about 1000 angstroms.

11. (currently amended) A method for forming a field effect transistor (FET) device comprising:

providing a semiconductor substrate;

forming over the semiconductor substrate to cover and define a channel region within the semiconductor substrate a gate electrode; and

forming within the semiconductor substrate and separated by the channel region within the semiconductor substrate a pair of source/drain regions, wherein an interface of the channel region covered by the gate is corrugated, said corrugated interface comprising rounded valley bottom portions and peak portions.

12. (currently amended) A method for forming a field effect transistor (FET) device comprising:

providing a semiconductor substrate;

forming over the semiconductor substrate to cover and define a channel region within the semiconductor substrate a gate

electrode; and

forming within the semiconductor substrate and separated by the channel region within the semiconductor substrate a pair of source/drain regions, wherein an upper surface of the gate electrode is corrugated, said corrugated surface comprising rounded valley bottom portions.

13. (original) The method of claim 8 wherein both the interface of the channel region covered by the gate electrode and the upper surface of the gate electrode are corrugated, said corrugated interface and said corrugated surface comprising rounded valley bottom portions and rounded peak portions.

14. (previously presented) The method of claim 8 wherein the gate electrode is formed to a thickness of from about 500 to about 2000 angstroms.

15. (previously presented) The field effect transistor (FET) device of claim 1 wherein the semiconductor substrate comprises materials selected from the group consisting of silicon and compound semiconductors.

16. (previously presented) The field effect transistor (FET) device of claim 4 wherein the semiconductor substrate comprises materials selected from the group consisting of silicon and compound semiconductors.

17. (previously presented) The field effect transistor (FET) device of claim 5 wherein the semiconductor substrate comprises materials selected from the group consisting of silicon and compound semiconductors.

18. (previously presented) The method of claim 8 wherein the semiconductor substrate comprises materials selected from the group consisting of silicon and compound semiconductors.

19. (previously presented) The method of claim 11 wherein the semiconductor substrate comprises materials selected from the group consisting of silicon and compound semiconductors.

20. (previously presented) The method of claim 12 wherein the semiconductor substrate comprises materials selected from the group consisting of silicon and compound semiconductors.